IN THE CLAIMS:

1. (Original) A programmable metal-oxide-semiconductor (MOS) memory circuit comprising:

a latch module having a first output and a second output based on a voltage difference between a first input and a second input;

a first N-type transistor having a gate region tied with a drain region and connectable to a first control voltage level, and a source region connected to a second control voltage level;

a second N-type transistor having a gate region tied with a drain region and connectable to the first control voltage level, and a source region connected to the second control voltage level; and

a connection module for connecting the drain region of the first N-type transistor to the first input, and the drain region of the second N-type transistor to the second input,

wherein the first and second control voltage levels are imposed to program either the first or second N-type transistor by causing a voltage difference between the drain region and the source region (Vds) and voltage difference between the gate region and the source region (Vgs) to be bigger than an operating voltage to induce a hot carrier effect, and

wherein the first and second outputs of the latch produce voltage results representing whether the first or second N-type transistor has been programmed when the connection module is enabled.

2. (Currently Amended) The circuit of claim 1 wherein the first <u>control</u> voltage level is imposable through a P-type transistor to the drain region of the first or second N-type transistor.

3. (Original) The circuit of claim 2 wherein the first and second N-type transistors have thinner gate oxide layers than that of the P-type transistor.

4. (Original) The circuit of claim 1 wherein the first control voltage level is higher than the operating voltage.

5. (Original) The circuit of claim 1 wherein the second control voltage level is at a ground level.

6. (Original) The circuit of claim 1 wherein the first and second N-type transistors are thin gate oxide transistors.

7. (Original) The circuit of claim 1 wherein the first or second output of the latch is complementary to the other.

8. (Original) The circuit of claim 1 wherein the connection module has two N-type transistors with their gates connected together to a third control voltage level.

9. (Currently Amended) The circuit of claim 8 wherein the N-type transistors are thick gate oxide MOS devices.

10. (Currently Amended) A method for programming a metal-oxide-semiconductor (MOS) memory circuit, the circuit comprising a latch module having a first input and a second input and one or more outputs, a first and second N-type transistors each having its gate region tied with its respective drain region which is connectable to a first control voltage level and their source regions connected to a second voltage level, and a connection module for connecting the drain region of the first N-type transistor to the first input, and the drain region of the second N-type transistor to the second input, the method comprising:

disenabling the connection module for disconnecting the drain region of the first N-type transistor from the first input, and the drain region of the second N-type transistor from the second input;

imposing the first control voltage level on the drain and gate regions of the first or second N-type transistor; and

relieving the first control voltage from the connected drain and gate regions of the first or second N-type transistor.

11. (Original) The method of claim 10 further comprising generating one or more voltage results from the outputs of the latch representing whether the first or second N-type transistor has been programmed.

12. (Original) The method of claim 11 wherein the generating further includes:

enabling the connection module for connecting the drain region of the first N-type transistor to the first input, and the drain region of the second N-type transistor to the second input; and

generating a first voltage result representing that the first or second N-type transistor has been programmed by comparing the voltage difference between the first input and the second input.

13. (Original) The method of claim 10 wherein the first control voltage level is imposable through two thick gate oxide P-type transistors to the drain region of the first and second N-type transistors wherein the gate oxide layers of the N-type transistors are thinner than the P-type transistors.

14. (Currently Amended) The method of claim 10 wherein the first control voltage level is higher than an operating voltage of the latch.

15. (Currently Amended) The method of claim 10 wherein the second control voltage level is at a ground level.

16. (Original) A programmable thin gate oxide N-type MOS memory device comprising:

a gate region tied with a drain region and connectable to a first control voltage level;

a source region connected to a second control voltage level,

wherein the first and second control voltage levels are imposed to cause a voltage difference between the drain region and the source region (Vds) and voltage difference between the gate region and the source region (Vgs) of the device to be bigger than a predetermined threshold voltage to cause a hot carrier effect for increasing the resistance thereof so that the device functions as a one-time programmable fuse.

17. (Original) The device of claim 16 wherein the first control voltage level is 3.3V.

18. (Original) The device of claim 16 wherein the threshold voltage is 1.2V.

19. (Original) A programmable metal-oxide-semiconductor (MOS) memory circuit comprising:

a first N-type thin gate oxide transistor having a gate region tied with a drain region and connectable to a first control voltage level, and a source region connected to a second voltage level; and

a second N-type thin gate oxide transistor having a gate region tied with a drain region and connectable to the first control voltage level, and a source region connected to the second voltage level,

wherein the first and second control voltage levels are imposed to program either the first or second N-type thin gate oxide transistor by causing a voltage difference between the drain region and the source region (Vds) and voltage difference between the gate region and the source region (Vgs) to be bigger than a predetermined threshold voltage to induce a hot carrier effect.

20. (Original) The circuit of claim 19 further comprising:

a latch module having a first output and a second output based on a voltage difference between a first input and a second input,

wherein the first and second inputs are connectable to the drain regions of the first and second N-type thin gate oxide transistors to generate the first and second outputs of the latch representing whether the first or second N-type thin gate oxide transistor has been programmed..

21. (Original) The circuit of claim 20 further comprising a connection module having two N-type thick gate oxide transistors with their gates connected together to a third control voltage for connecting the drain region of the first N-type thin gate oxide transistor to the first input of the latch, and the drain region of the second N-type thin gate oxide transistor to the second input of the latch.

22. (Original) The circuit of claim 19 further comprising a P-type thick gate oxide transistor connecting the first voltage level to the drain region of the first or second N-type thin gate oxide transistor.

AMENDMENTS TO THE DRAWINGS

The attached sheet of drawing includes changes to Fig. 3A. This sheet, which includes Fig. 3A-3B replaces the original sheet including Fig. 3A-3B. In Figure 3A, a typographical error has been corrected.